Novel BiCMOS Compatible, Short Channel LDMOS Technology for Medium Voltage RF & Power Applications

[1]Andrej Litwin, [2]Olof Bengtsson, and [3]Jörgen Olsson

[1]Ericsson Microelectronics, SE-164 81 Kista, Sweden, [2]Swedish Linear Microwave, SE-802 67 Gävle, Sweden, [3]Uppsala University, SE-751 21 Uppsala, Sweden

Abstract — **We describe a very short channel, 0.15 μm, LDMOS transistor, with a breakdown voltage of up to 45 V, manufactured in a standard 0.35 μm BiCMOS process. At 1900 MHz and a 12V supply voltage the 0.4mm gate width device gives 100 mW output power $P_{1\,dB}$ at a drain efficiency of 43%. It has a transducer power gain of more than 20dB and a current gain cutoff frequency, f_T, of 13 GHz. The maximum available gain cutoff frequency, f_{MAX}, is 27 GHz. The LDMOS process module does not affect the performance or models of other devices. We present for the first time a simple way to create high voltage, high performance LDMOS transistors for RF power amplifier use even in a very downscaled silicon technology.**

I. Introduction

The ever-increasing market for digital basestation power amplifiers in PCS, CDMA, and WCDMA systems *requires low cost, ease of use technology which* can provide high power and good linearity performance. LDMOS started replacing bipolar devices in basestation applications 3-4 years ago and has for multiple reasons become the leading technology for basestation power amplifier applications. It has high gain and shows excellent back-off linearity. The breakdown voltage BV_{dss} can be easily adjusted by layout to fit different application voltages. The integration of LDMOS transistors into a RF BiCMOS process [1], including the necessary passive components, provides a tool for design of monolithic silicon amplifiers with sensing and control circuitry onboard. More important, it also opens the way to more efficient linear RF power amplifiers with integrated linearization circuits on the same die. The output power of such integrated PA should be in the 10 W range, with power supply of 10-12 V, requiring LDMOS transistors with a breakdown voltage higher than 30 V. This paper describes a very short channel, high performance, LDMOS structure, simple to integrate with conventional CMOS/BiCMOS and not affecting the other devices, it's processing, DC and AC performance.

II. Device Design and Fabrication

The LDMOS transistor was implemented in a standard 0.35 μm BiCMOS process adapted for RF applications. The LDMOS process required only one extra implantation mask, with no additional heat treatment, thus not affecting the performance and models of other devices. The implantation was performed as a pocket implant [2] of boron at an angle of 30° to provide the necessary LDMOS p-well (p-body) surrounding the source diffusion, see Fig. 1 for transistor structure. The resulting channel length of the transistor was approximately 0.15 μm, according to Athena process simulation. The gate oxide in the channel region was the same as for the other CMOS transistors, i.e. 6.7 nm. The birds beak encroachment from the field oxide covering the extended drain was approximately 0.1μm, see transistor cross-section in Fig. 2, leaving only the distance of 0.3 μm between the gate edge and the thick field oxide. The process used Ti salicide to reduce the series resistance on both polysilicon gates and source/drain areas, but also to strap the source n+ diffusion to the p+ body contact. The process has an option of deep metal plugs that make it possible to strap the source regions of the LDMOS transistors to a p+ substrate [3].

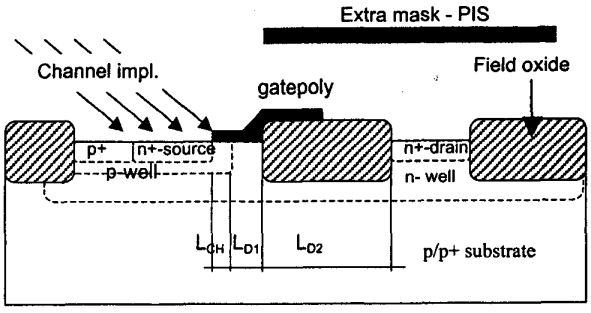

Fig. 1. LDMOS devices structure dimensions after processing: L_{CH} = 0.15 μm, L_{D1} = 0.15 μm, L_{D2} = 1.2 - 2.4 μm (different layouts).

0-7803-7239-5/02/$10.00 © 2002 IEEE

The transistor layout was optimized for both high voltage and high frequency performance. The transistors were designed as multi-finger devices with 20 μm gate width of each finger. The drain was enclosed by the gate to minimize both C_{ds} and to avoid fringing fields, reducing the breakdown voltage. The extended drain region, separating the channel region from the drain contact, was covered by thick field oxide, reducing both C_{gd} and increasing significantly the possible V_{gd} before oxide breakdown.

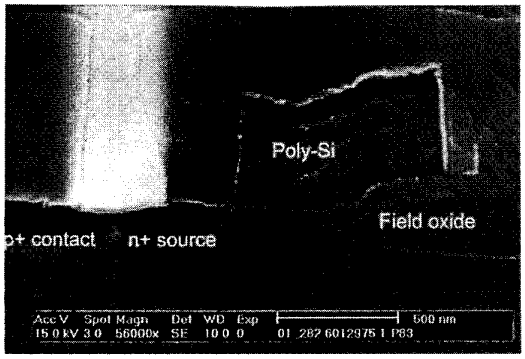

Fig. 2. The LDMOS transistor cross-section from the source side.

III. DC PERFORMANCE

Transistors were manufactured with three different extended drain regions: 1, 1.5 and 2.2 μm (mask dimension). The breakdown voltage BV_{ds} is approximately 35, 40 and 45 V, respectively. The breakdown is limited by the high field at the corners of the drain region, observed by emission microscopy. The series resistance R_{ds} in the linear region of the I-V characteristics is also affected by the size of extended drain region, varying almost a factor of 2 for the shortest and longest device. The maximum available drain current I_{ds} is over 50 mA at a V_{gs} of 3.5 V for the devices with 0.4 mm total gate width and almost independent of the length of the extended drain region. Since the transistors with the extended drain region of 1 μm have high enough breakdown voltage for the application, the following data address these devices. An example of the I - V characteristics of the transistor are presented in Fig. 3.

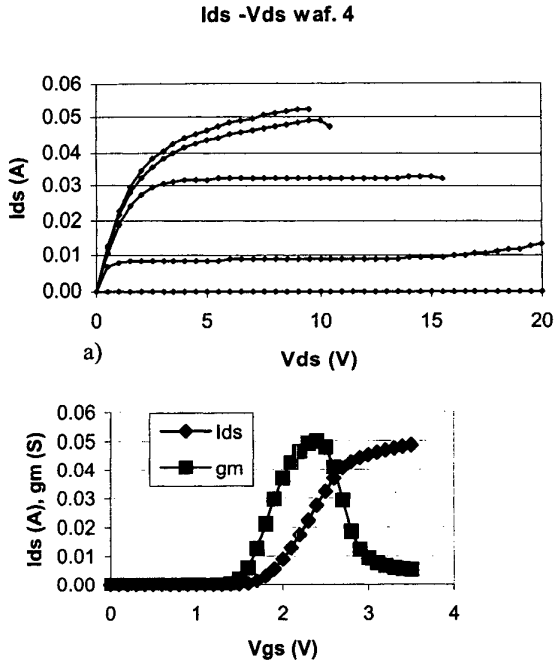

Fig. 3. I - V characteristics of LDMOS transistor with a total gate width of 0.4 mm, and extended drain region of 1μm a) I_{ds} vs. V_{ds} for V_{gs} = 1 - 3.5 V in 0.5 V steps, b) I_{ds} & gm vs. V_{gs} at V_{ds} = 6 V, V_{th} = 1.8 V

IV. SMALL SIGNAL AC PERFORMANCE

Small signal s-parameters were measured on wafer with a standard 150 μm pitch ground-signal-ground probe calibrated and de-embedded for pad capacitances. The current gain, h_{21}, was calculated and the current gain cutoff frequency, f_T, extracted. Maximum f_T was found to be 13 GHz. The maximum power gain cutoff frequency f_{MAX} = 27 GHz was extrapolated from the MAG measurements at 12 V DC supply voltage and 18 mA drain current, Fig. 4. The bias dependence of f_T and f_{MAX} i

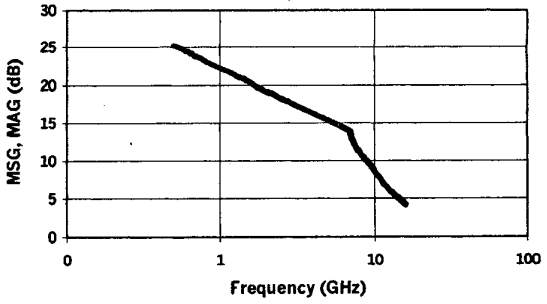

Fig. 4. Small signal MSG and MAG versus frequency at 12V DC supply voltage and 18mA drain current.

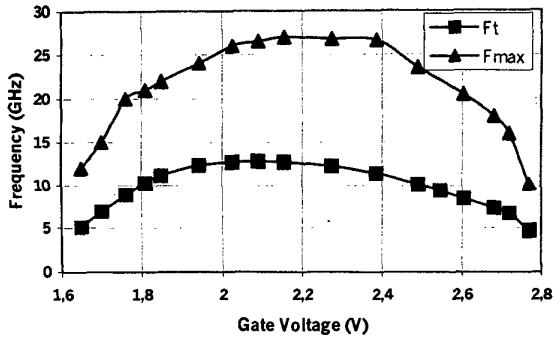

Fig. 5. Current gain and maximum available gain cutoff frequencies versus gate voltage at 12 V DC supply voltage. Highest value of f_{MAX} coincide with the bias for highest gm, while maximum f_T is achieved for somewhat lower bias.

V. Power Performance

Power evaluation was made using a Maury Automated Tuner System, ATS, at the probe interface with probe tips calibrated using a standard calibration substrate. No de-embedding was done. Single tone excitation at 1.9 GHz shows very high transducer power gain, Gt, of more than 20 dB and a reasonable output power of 100 mW (20 dBm) at the 1 dB compression point. The drain efficiency at that point is 43% and reaches a maximum of 46% further into compression, Fig. 6.

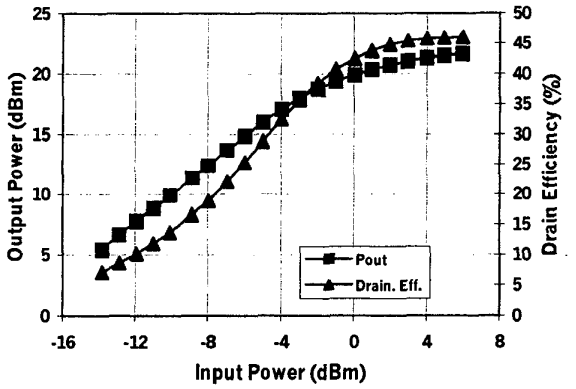

Fig. 6. Output power and drain efficiency versus input power at 1.9 GHz, 12 V DC supply voltage and 3 mA quiescent drain current.

The device shows high power gain also for higher frequencies, Fig. 7, in line with the low roll off rate of the small signal MSG, -10 dB per decade until the breakpoint is reached [4] and [5]. At 3.0 GHz the device still shows an extremely high transducer power gain of more than 20dB but the drain efficiency has gone down to 20 percent with an output power of 30mW (15dBm) at the 1 dB compression point.

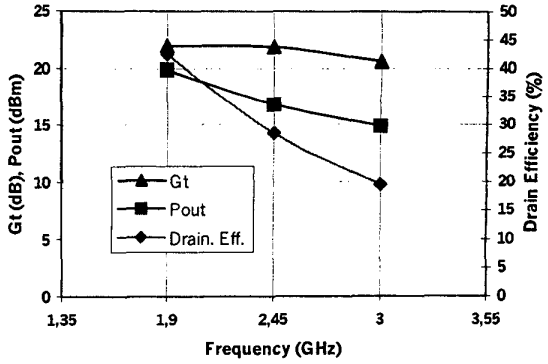

Fig. 7. Gain, output power and drain efficiency at the 1 dB compression point versus frequency for 12 V DC supply voltage and 3 mA quiescent drain current

The gain is very bias dependent, as shown is Fig. 8. The graph shows a maximally flat gain at a quiescent drain current of 3 mA, a low class AB bias point. The 1 dB output power compression point increases from 17 dBm to 19 dBm going from class A to class AB but at the expense of approximately 2 dB lower gain as expected [6].

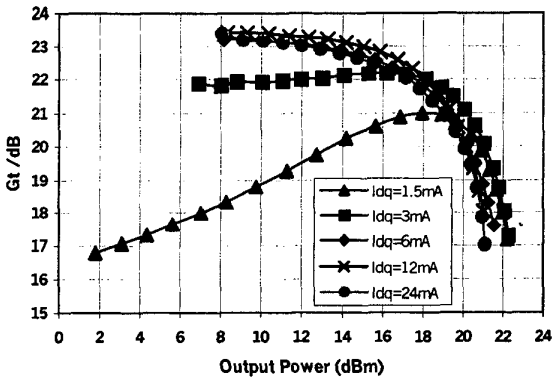

Fig. 8. Gain versus output power and quiescent drain current at 1.9GHz and 12V DC supply.

VI. Two-tone Power Performance

Evaluation of two-tone intermodulation distortion, IMD, was performed in the same measurement set up as in the section above. The measurement results of the device at 1.9 GHz are shown in Fig. 9 and Fig. 10. For the

maximally flat gain, at a quiescent drain current of 3 mA, the 3'rd order IMD is -20 dBc at a peak envelope output power, PEP, of 21 dBm, Fig 9. When backed-off to 3'rd order IMD less than -30 dBc, the PEP output drops to 17.5 dBm at the optimum bias of 6 mA, Fig. 10.

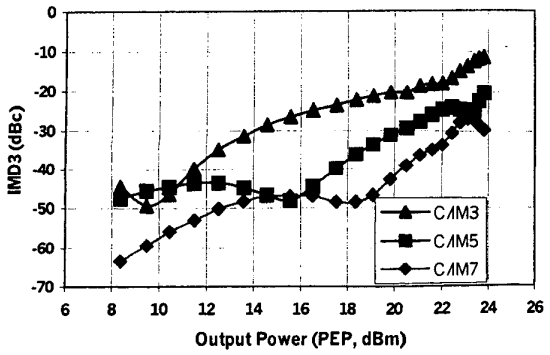

Fig. 9. Two-tone intermodulation distortion versus peak envelope output power at 12 V DC supply voltage and 3mA quiescent drain current. f1=1.9000 GHz, f2=1.9001 GHz.

The IMD3 values versus bias show a substantial bias sensitivity resulting in a maximum difference of more than 10 dB in the backed-off region used in modern telecommunications systems, with high peak to average.

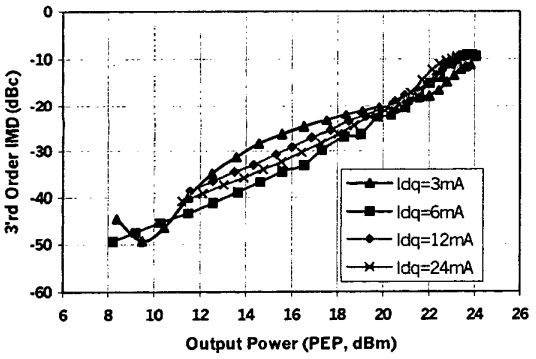

Fig. 10. Two-tone 3'rd order intermodulation distortion, IM3 versus peak envelop output power for different bias points at 12 V DC supply voltage. f1=1.9000 GHz, f2=1.9001 GHz.

V. Conclusion

We have described a high frequency, high voltage LDMOS transistor, incorporated in a standard CMOS/BiCMOS process. Since this addition does not affect the performance of other devices, the reuse of old design blocks is possible without any major changes. The measured RF-power and distortion behavior meet the requirements for integrated power amplifiers for supply voltage 10 - 12 V. The results also indicate that operation could be extended up to a few GHz range, subject of current investigations. The on wafer measurements cannot be directly compared to the demands placed on packaged devices by modern communication standards and designed for higher supply voltage [7]. The measurement results show higher gain and reduced IMD performance in comparison to packaged transistors with internal matching.

Acknowledgement

The authors wish to acknowledge Ericsson Radio Access AB, Kista and especially Zoran Draganic for fruitful measurement discussions and for making the power measurements possible at their facilities.

References

[1] Y. Tan, M. Kumar, J. Cai, and J. K. O. Sin, "A SOI LDMOS technology compatible with CMOS, BJT, and passive components for fully-integrated RF power amplifiers", *IEEE Trans.Electron Devices*, vol. 48, pp. 2428-2433, Oktober 2001.

[2] Puchner-H; Aronowitz-S; Kimball-J " Impact of pocket implant and channel interface modeling on the reverse short channel effect" Proceedings of the 28th European Solid-State Device Research Conference, Paris, France; 1998; p.116-19

[3] T. Johansson, "Wireless-Trench Technology: A new approach to grounding in integrated power amplifiers", presented at the GHz2001 Symposium, Nov. 26-27 (2001), Lund, Sweden

[4] L. Vestling, L. Bengtsson, and J. Olsson, "A CMOS compatible power MOSFET för low voltage GHz operation", *1999* Proceedings of the IEEE European Microwave Conference, Vol. 2, pp. 21-24 , 1999.

[5] N. Rorsman, J. Olsson, C. Fager, L. Vestling, J. Ankarcrona, H. Zirath, and K.-H. Eklund, "High Voltage LDMOS Transistors for Increasing RF Power Density and Gain", presented at the GHz2001 Symposium, Nov. 26-27 (2001), Lund, Sweden

[6] S. C. Cripps, *Rf power amplifiers for wireless communications*, London: Artech House, 1999.

[7] A. Litwin, Q. Chen, J. Johansson, G. Ma, L. A. Olofsson and P. Perugupalli, "High power LDMOS technology for wireless infrastructure", Conf. Proc. GAAS 2001, Sept. 2001, London, UK